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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,782	08/22/2003	Keiichiro Kata	069974-0143	8077
22428	7590 02/14/2005		EXAMINER	
FOLEY AND LARDNER			PRENTY, MARK V	
SUITE 500				
3000 K STREET NW			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20007			2822	

DATE MAILED: 02/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

			$\mathcal{O}_{\mathcal{I}}$		
		Application No.	Applicant(s)		
Office Action Summary		10/645,782	KATA ET AL.		
	Office Action Summary	Examiner	Art Unit		
		MARK V. PRENTY	2822		
- Period fo	 The MAILING DATE of this communication appropriate the property 	pears on the cover sheet with the c	correspondence address		
THE N - Extense after S - If the p - If NO p - Failure Any re	PRTENED STATUTORY PERIOD FOR REPL MAILING DATE OF THIS COMMUNICATION. sions of time may be available under the provisions of 37 CFR 1 SIX (6) MONTHS from the mailing date of this communication. Deriod for reply specified above is less than thirty (30) days, a rep- period for reply is specified above, the maximum statutory period to reply within the set or extended period for reply will, by statute toply received by the Office later than three months after the mailing at patent term adjustment. See 37 CFR 1.704(b).	I36(a). In no event, however, may a reply be tirely within the statutory minimum of thirty (30) day will apply and will expire SIX (6) MONTHS from e, cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. CD (35 U.S.C. § 133).		
Status					
1)⊠	Responsive to communication(s) filed on <u>22 A</u>	lugust 2003.			
·		s action is non-final.			
	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.				
Dispositio	on of Claims				
5)⊠ (6)⊠ (7)⊠ (Claim(s) <u>1-32</u> is/are pending in the application (a) Of the above claim(s) is/are withdra Claim(s) <u>2-8,10-12,15,16,26-28 and 30-32</u> is/a Claim(s) <u>17-20</u> is/are rejected. Claim(s) <u>1,9,13,14,17,21-25 and 29</u> is/are objection(s) are subject to restriction and/o	wn from consideration. are allowed. ected to.			
Application	on Papers				
9)□ T	The specification is objected to by the Examine	er.			
10)⊠ The drawing(s) filed on <u>22 August 2003</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.					
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
	Replacement drawing sheet(s) including the corrective oath or declaration is objected to by the E		• • •		
Priority u	nder 35 U.S.C. § 119				
a)[∑	Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority document as: 2. Certified copies of the priority document as: 3. Copies of the certified copies of the priority document application from the International Burea	ts have been received. ts have been received in Applicati nity documents have been receive	ion No. <u>08/533,207</u> .		
* S	ee the attached detailed Office action for a list	1 "	ed.		
Attachment(s)				
2) Notice 3) Inform	of References Cited (PTO-892) of Draftsperson's Patent Drawing Review (PTO-948) ation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) No(s)/Mail Date <u>3 of them</u> .	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal F 6) Other:			

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Art Unit: 2822

This Office Action is in response to the papers filed on August 22, 2003.

Independent claim 1 is objected to because it recites the "a plurality of chip electrodes positioned on said chip section" limitation twice. Correction is required. Claims 9, 13, 17, 21, 25 and 29 depend on independent claim 1 and are therefore similarly objected to.

Claim 9 is further objected to because it does not further limit claim 1.

Claims 13 and 14, which depend on independent claims 1 and 2, respectively, are objected to because they do not further limit claims 1 and 2. Specifically, independent claims 1 and 2 recite, "said interconnection layers extend from said periphery toward said center," and claims 13 and 14 do not further limit claims 1 and 2 in reciting, "wherein the plurality of chip electrodes are positioned on said periphery," because claims 1 and 2's "said interconnection layers extend from said periphery toward said center" means that one end of the interconnection layer is connected to the (periphery) chip electrode and the rest of the interconnection layer extends inwardly (see the specification at column 6, lines 60-67).

Claims 21-24, which depend on independent claims 1-4, respectively, are objected to because they do not further limit claims 1-4. Specifically, independent claims 1-4 recite, "said bump electrodes being located at positions other than over said chip electrodes," (i.e., the bump electrodes do not overlap the chip electrodes), and claims 21-24 do not further limit claims 1-4 in reciting, "wherein said bump electrodes do not overlap said chip electrodes."

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Claims 17-20 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. Specifically, claims 17-20 are inconsistent with

independent claims 1-4, on which they respectively depend. More specifically,

independent claims 1-4 recite, "said bump electrodes being located at positions other

than over said chip electrodes," but dependent claims 17-20 inconsistently recite:

"wherein said bump electrodes overlap said chip electrodes."

Claims 2-8, 10-12, 15, 16, 26-28 and 30-32 are allowable over the prior art of

record.

Independent claims 1 and 2 remain allowable over the prior art of record for the

reason they were first allowed. Specifically, the prior art of record does not disclose or

suggest the claimed semiconductor wafers taken as a whole, including the bump

electrodes being located at positions other than over the chip electrodes (i.e., the bump

electrodes do not overlap the chip electrodes), and the interconnection layers extending

from the (chip electrodes positioned on the) chip section periphery inwardly toward the

chip section center.

United States Patent 5,844,304 is related to this application.

Registered practitioners can telephone the examiner at (571) 272-1843. Any

voicemail message left for the examiner must include the name and registration number

of the registered practitioner calling, and the Application/Control (Serial) Number.

Technology Center 2800's general telephone number is (571) 272-2800.

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